Signal Integrity Evaluation of a 10 Gbits/sec Optoelectronic interconnect

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Abstract **Signal integrity is of vital importance to high speed interconnects. The *10G* system is a 10 Gbit/second optical interconnect with a cross-section bandwidth of over 1T bit/second fabricated on a heterogeneous platform consisting of a multi-chip module, high-speed SiGe and GaAs opto-electronics. . We compare lumped and multisegment microstrip models of the transmission lines on the MCM hybrid. We also modeled the wirebonds using a Quasi-Static model and a Co-Planar Waveguide (CPW) model for the bump bonds between the GaAs and SiGe substrates. These models are utilized by a behavioral simulator to demonstrate the effects of interconnect components on waveform shape. The results demonstrate convincingly that signal integrity is of critical importance to end-to-end performance measures at high transmission speeds and that incorporating these models is important to behavioral simulation.**

I. Introduction

The *10G[1]* system is a complex electro-optical interconnect that presents many challenges to a simulation environment. In this paper, we demonstrate how a Mixed Signal Mixed Domain simulator can be used for design verification of opto-electronic interconnects with particular attention to the role of passive components in the interconnect structure.

We begin by describing the *10G* system. Next, we pay particular attention to the role of the passive components in the interconnect including the transmission lines, bond wires and bump bonds and their effect on signal integrity. Lastly, we demonstrate the effect of passive interconnects on end-to-end system level performance through the use of a Mixed-Signal, Mixed-Domain simulator.

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II. Signal paths in The 10G System

One of the signal paths in the *10G* system is shown in Figure 1.

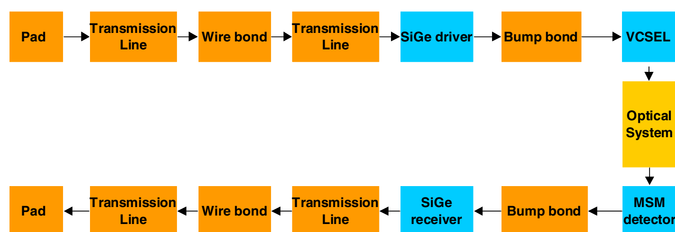

Figure 1. 10G Asynchronous Link Transmission Path

As shown, the incoming digital stream is connected to a pad on the edge of a Multi-Chip Module (MCM) shown in Figure 2. This pad is connected to a long transmission line that ends at a chip well for the Smart Pixel Array (SPA) SiGe/GaAs hybrid. A wire bond from the MCM signal layer is connected to the SiGe die. A short transmission line on the SiGe chip connects the pad to a driver/amplifier. A bump bond connects the SiGe substrate to the GaAs chip. On the GaAs substrate, a Vertical Cavity Surface Emitting Laser (VCSEL) emits light toward an offset lens system. The output of the lens reflects off the top mirror and back down to another lens. The output of the second lens is received by a Metal-Semiconductor-Metal (MSM) photodetector on the GaAs substrate, which is connected via another bump bond to the SiGe receiver, which is comprised of a transimpedance amplifier and a limiter. From this point to the output pad, the receive path is the reverse of the transmission path.

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III Passive Interconnect

A. Transmission Line

As shown in Figure 2, the MCM is a multi-layer laminate structure with ground and power planes interlaced throughout.[2][3][4]

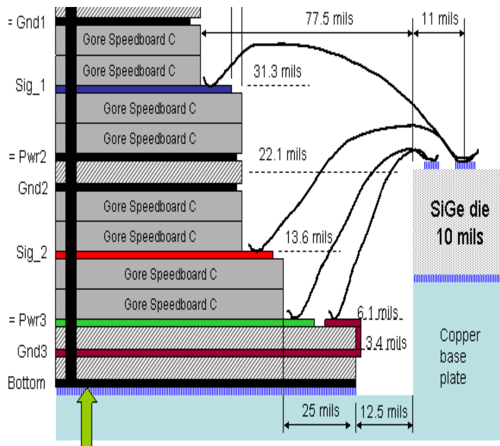

Figure 2 SPA Multilayer laminate structure

Treating the ground planes as reference, we can use the dielectric constant of the signal plane to find the characteristic impedance of the line. The transmission line can be modeled to different degrees of accuracy. The first model presented is a simple lumped model of the entire line while the second model is a multi-segment model.

The serpentine path of the asynchronous link signal trace can be obtained from a PCB layout tool. The first extraction of the asynchronous link (from pad to bond wire) is from the Cadence Allegro PCB tool; the output is shown in the data in Table 1.

Impedance : (min) 57.962 ohm, (max) 73.737 ohm
Inductance : 47.7713 nH
Capacitance : 14.1532 pF (to SHIELD LAYER)
Prop Delay : 0.822036 ns
Resistance : 377.546 mOhm
Capacitance : 6.55227 pF (to SIGNAL))

Table 1. Cadence Allegro lumped model output

Note that the impedance of the line has a maximum and minimum due to the particularly simple geometric model. We used the mean of these values as the line impedance. To form a lumped model, we constructed a π equivalent differential model shown in Figure 3. This can be simulated using a time-domain electrical simulator, such as Spectre-RF™ as shown in Figure 4.

Using the multi-segment geometric data, the transmission line can be converted into a model suitable for either a multi-segment lumped model or a three-dimensional full-wave finite-element simulation. In either case, the resulting scattering parameters can provide a frequency dependent view of the line.

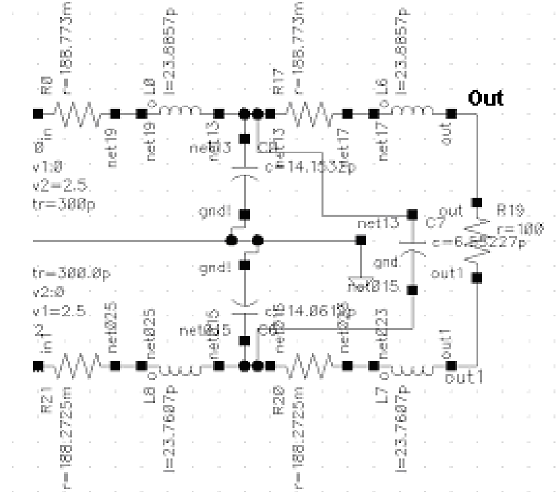

Figure 3. Transmission line lumped model schematic

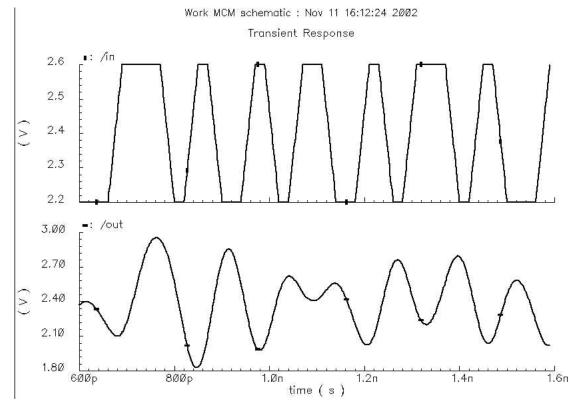

Figure 4. Spectre-RF lumped model input and output

The results from the multi-segment microstrip model are shown in Figure 5. Using this model in Agilent's ADS, the simulation of insertion loss benefits very little from the added complexity in the line model, though it is seen that the reflections decay sooner with the complex model.

Using full wave modeling (such as Finite Difference Time Domain (FDTD) or Method of Moments (MoM) for the transmission line is a possibility. However, in a behavioral simulator, these methods are neither fast enough for interactivity or convenient due to the meshing requirement. Furthermore, the frequency domain output must be converted to a time domain model for use in a time domain SPICE-like simulator.

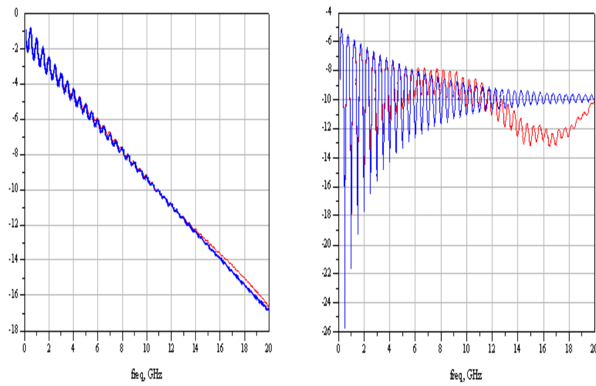

Figure 5. Transmission line simulation using ADS (insertion loss [Left] Return loss [Right])

B. Wire Bonds

At microwave frequencies, wire bonds begin to affect signal integrity. There are two methods for modeling the bond wires: (1) Mesh the wire and apply full wave methods like FDTD[6] or MoM[7] to calculate the S-parameters (2) Use a quasi-static model. The second approach turns out to be easier and just as accurate. Alimenti, et al.[8][9] propose a simple model as follows: divide the bond wire into two halves; then divide each half into three regions: the pad, the wire over the substrate and then the wire over the ground plane.

The pad is treated as a T subcircuit, the other two regions as lossless transmission lines. The computation of the length of the transmission lines is computed by assuming that the bond wire is a radial chord. The T subcircuit parameters are computed from lumped circuit assumptions. The input parameters for the model of Alimenti, et al. were found by detailed examination of the MCM cross section in Figure 2. The component values for the equivalent T subcircuits and transmission line parameters were computed by a separate tool. Table 2 gives the actual input parameters given to the tool derived by visual inspection of Figure 2.

Because of the differing dielectrics, the impedances (Z0) of the four transmission lines and the normalized length (NL) are different, as expected. Using a 10 GHz input, the time domain response of the bond wire can be seen in Figure 6. The distortion of the input waveform can be easily seen. (Note that the wider pulses result from wider inputs)

W1	76.3	3 mil width
H1	795	31.3 mils
P1	254	10 mil pad
D1	76.2	3 mil separation
Eps1	4.4	
W2	254	10 mils
H2	561	22.1 mils high
P2	61	
D2	76.2	
Eps2	11.825	SiGe
hb	895	H1+4 mil height
g	317	12.5 mil gap
dw	25.4	1 mil wire

Table 2. Bond wire parameters

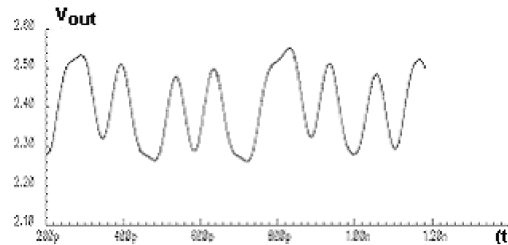

Figure 6. Spectre-RF bond wire simulation output

C. Bump Bonds

The bump bond is the "joint" between the SiGe substrate and the GaAs optoelectronics. Bump bonds have been shown to be of great utility in microwave applications however they present an impedance discontinuity between substrates due to parasitic reactance. Deriving an equivalent circuit for the solder bump is difficult, because it is hard to de-embed the bump from the substrates. One strategy is to use "Design of Experiments"[12] to obtain the equations for the components of the model. This was the approach taken by Staiculescu, et al[13]. They modeled the conductor on the substrate as a Co-Planar Waveguide (CPW) and used a standard π model. Using the CPW bump bond model, the following input parameters (all in mils, shown in Table 3) generates SPICE compatible output directly usable by the simulator

Table 3. Solder bump parameters

Bump height	20
Conductor overlap	120
Width of line	150
Bump diameter	30
Distance to ground plane edge	50

Using the Spectre-RF™ simulator, the time domain response of the solder bump can be simulated. There is only a little distortion evident in the waveform output.

III. SYSTEM LEVEL SIMULATION

While simulators like Spectre-RF™ are useful for evaluating small sections of the design, they are incapable of handling system level simulations due to (1) large computational requirements and (2) the mixed signal environment. With a system level simulator, the parameters of models can be changed and the simulations re-run. Because these are higher level models, the simulation time is on the order of seconds, not hours. For example, an end-to-end simulation can be run on the entire system with the performance results of the whole system, so the designer can get fast evaluation of the feasibility of the design under consideration. The system level simulator *Chatoyant[5][14],* can be used to generate graphical measures of system performance, such as eye diagrams. Additionally, quantitative measures such as Bit Error Rate (BER) are calculated through statistical estimation.

Using the models discussed previously, we can simulate the asynchronous link "end-to-end". We can see the eye openings with a 2.5 GHz input (shown in Figure 7). At 5.0 GHz, the eye opening significantly degrades as shown in Figure 8.

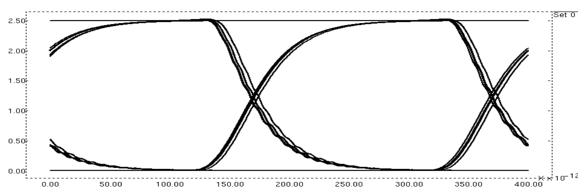

Figure 7. Eye opening at 2.5 GHz

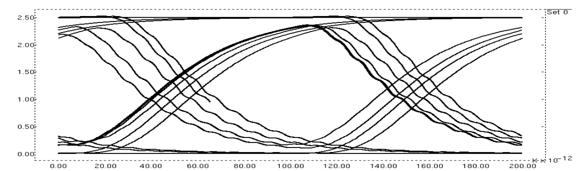

Figure 8. Eye opening at 5.0 GHz

IV. CONCLUSION

System level designers use behavioral simulators to evaluate the design tradeoffs. We have shown that passive interconnects must also be effectively modeled when the system is expected to perform at high speeds. The results demonstrate convincingly that signal integrity is of critical importance to system level at high transmission speeds and that incorporating these models is equally important to behavioral simulation. Furthermore, simple lumped and Quasi-Static models suffice to provide useful information to the designer at the system level.

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